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IN THE CLAIMS

Presented below is a complete listing of claims.

1. (Previously presented) A method, comprising:

providing a first resistor with a first end and a second end, said first end coupled to a switch and said second end coupled to a serial data bus wire at a near end of a serial data bus;

controlling said switch with a detach control signal sent on a detach control signal wire separate from data transmission wires of said serial data bus from a far end of said serial data bus to cause an apparatus containing said first resistor and said switch to enter a logically detached state;

influencing said detach control signal with a wake-up signal sent on a wake-up signal wire separate from said data transmission wires of said serial data bus from said near end of said serial data bus to said far end of said serial data bus; and

switching a biasing voltage from said resistor utilizing said switch.

2. (Canceled)

3. (Original) The method of claim 1, wherein said first resistor is configured as a pull-up resistor.

4. (Original) The method of claim 3, further comprising detecting said switching of said biasing voltage.

Assignee: Intel Corporation

5. (Original) The method of claim 4, further comprising determining a logically detached state responsive to said detecting.

6. (Canceled)

7. (Previously presented) The method of claim 1, wherein said detach control signal is asserted when said wake-up signal is de-asserted.

8. (Previously presented) An apparatus, comprising:
a first resistor with a first end and a second end;
a switch coupled to said first end of said first resistor and to a bias voltage;
a detach control signal wire separate from data transmission wires of a serial data bus coupled to said switch at a near end of said serial data bus, to receive a detach control signal sent from a far end of said serial data bus to cause said apparatus to enter a logically detached state;
a wake-up signal wire separate from said data transmission wires of said serial data bus to send a wake-up signal from said near end of said serial data bus to said far end of said serial data bus to influence said detach control signal; and
a serial data bus wire of said serial data bus coupled to said second end of said first resistor.

Assignee: Intel Corporation

9. (Previously presented) The apparatus of claim 8, wherein said switch may apply said bias voltage to said first end of said first resistor responsively to said detach control signal on said detach control signal wire.

10. (Previously presented) The apparatus of claim 9, wherein said detach control signal is asserted when said wake-up signal is de-asserted.

11. (Previously presented) The apparatus of claim 8, wherein said serial data bus carries universal serial bus data.

12. (Previously presented) The apparatus of claim 8, wherein said serial data bus carries IEEE-1394 bus data.

13. (Previously presented) The apparatus of claim 8, further comprising a second resistor with a first end and a second end, said first end coupled to said serial data bus wire.

14. (Previously presented) The apparatus of claim 13, wherein said second end of said second resistor is coupled to signal ground.

Assignee: Intel Corporation

15. (Previously presented) An apparatus, comprising:

means for providing a first resistor with a first end and a second end, said first end coupled to a switch and said second end coupled to a serial data bus wire at a near end of a serial data bus;

means for controlling said switch with a detach control signal sent on a detach control signal wire separate from data transmission wires of said serial data bus from a far end of said serial data bus to cause said apparatus to enter a logically detached state;

means for influencing said detach control signal with a wake-up signal sent on a wake-up signal wire separate from said data transmission wires of said serial data bus from said near end of said serial data bus to said far end of said serial data bus; and

means for switching a biasing voltage from said resistor utilizing said switch.

16. (Canceled)

17. (Previously presented) The apparatus of claim 15, further comprising means for detecting said switching of said biasing voltage.

18. (Previously presented) The apparatus of claim 15, wherein said detach control signal is asserted when said wake-up signal is de-asserted.

Assignee: Intel Corporation

19. (Previously presented) A system, comprising:

a serial data bus with a near end and a far end;

a first circuit, coupled to said near end, including a first resistor with a first end and a second end, a switch coupled to said first end of said first resistor and to a bias voltage, a serial data bus wire of said data bus coupled to said second end of said first resistor, a detach control signal wire separate from data transmission wires of said serial data bus coupled to said switch to receive a detach control signal sent from said far end of said serial data bus to said near end of said serial data bus, and a wake-up control signal wire separate from said data transmission wires of said serial data bus to send a wake-up signal from said near end of said serial data bus to said far end of said serial data bus; and

a second circuit, coupled to said far end, to send said detach control signal responsive to said wake-up signal to cause said first circuit to enter a logically detached state.

20. (Previously presented) The system of claim 19, wherein said switch may apply said bias voltage to said first end of said first resistor responsively to said detach control signal.

21. (Previously presented) The system of claim 19, wherein said detach control signal is asserted when said wake-up signal is de-asserted.

22. (Canceled)